Preliminary

Specification for CMS QIE ASIC

Original
4/10/00
Revised
2/2/01

Revision History

Date	**Name**	
2/2/01	TMS	Added timing information for RESET

QIE overview and experience

QIE is an acronym for the functions of the ASIC, Q (charge) I (integration) and E (encode). A large dynamic range is accomplished through a multi-range technique. The input current is simultaneously integrated on all ranges, and comparators are used to select the lowest range that is not at full scale. The selected voltage representing the integrated charge is then put through an on-chip FADC. The outputs are a 5 bit mantissa representing the voltage and a two-bit code indicating the range. Operations are time multiplexed and pipelined to allow signals to settle and to make the reset interval the same as the integration interval. Latency is 100 ns as the pipeline is four clock cycles deep.

The current splitter design uses outputs which are X5, X1, X1 and X1 four each of the four possible ranges. The range weighting is done by ratioing the capacitor value of the integrating amplifiers for each range.

One set of capacitors integrates the input current for one beam crossing interval; the clock frequency is equal to the beam-beam collision frequency. While one set of capacitors is collecting charge, others are being read out and reset. There are four sets of capacitors. At any given point in time, one set is collecting charge, one is settling, one is being read out, and one is being reset.

A DC bias current is added to the input current. One of the functions of the bias current is to provide a minimum current in the splitter to ensure that the transistors are in a good operating region. For a given charge deposition over one clock interval, no more than one capacitor in the set will have its voltage within specified limits. The voltage on this capacitor is digitised by an on-board chip FADC. The priority encoded address of this capacitor make up the exponent bits. The voltage on the capacitor is the mantissa and the address of the capacitor is the exponent.

The QIE is presently in service on the 3100 channel KTeV caesium iodide crystal calorimeter. CsI has an intrinsic energy resolution approaching 0.5%, which requires very high performance electronics to make full use of this capability. The KTeV device has 8 ranges with a factor of two gain change between ranges giving a dynamic range of 16 bits. There are a number of distortions in the transfer function of this device. The main contributions to the non-uniformity in the overall charge to voltage slope are variations in the size of the capacitors and accuracy of the splitter. Although this is a less than 0.7% effect, KTeV keeps four sets of calibration factors for each QIE, which amounts to 64 constants, four sets of 8 slopes and 8 offsets.

General:

Power Dissipation < .6 Watts
Number of supply Voltages 2
Package: Thin Quad Flat Pack (TFQP)
Package Pins <=80
Pipeline stages = 4
Auto Range and Fixed Range Selectable
Pedestal adjust via external lines
Internal FADC (5 Bits) (Probably Non-linear)

Inputs:

Charge input (~50 Ohms)
Reference input (~50 Ohms)
QIE Clk (FADC Clk derived and timed internally)
Polarity Select
Pedestal Adjust
Range Select
Calibration Mode
Reset

Outputs:

Exponent – 2 bits
Mantissa – 5 bits
CapID - 2 bits
Note: All Outputs in sync for each Clock period.

Performance:

Clock Speed >40MHz
Must accept both polarity of charge input
    Positive Input gain relative to Negative Input = 2.67
Charge sensitivity Lowest Range = 1fC/LSB
    In Calibration Mode 1/3 fC/LSB Range 0 only Linear FADC
Maximum Charge = 9670 fC/25ns
Noise 1.5 LSBs in calibration mode, gaussian (Note: for Input Capacitance of ~ 70pF)
Nominal Pedestal
    Calibration Mode nominal Ped = 6.5
    Normal Data Mode Ped = .5
FADC Differential Non-Linearity < .05 LSBs

Proposed 4 Ranges and FADC codes for each range. Note: the FADC in Normal mode is piece-wise linear. In Calibration Mode Only Range 0 is active and it is linear over entire range.

Normal Mode			
Range (Exponent)	Input Charge	FADC Codes	Gain (q/Lsb)
0	-1 fC --- 14 fC	0---14	1 fC/bin
0	14 fC --- 28 fC	15---21	2 fC/bin
0	28 fC --- 40 fC	22---25	3 fC/bin
0	40 fC --- 52 fC	26---28	4 fC/bin
0	52 fC --- 67 fC	29---31	5 fC/bin
1	57 fC --- 132 fC	0---14	5 fC/bin
1	132 fC --- 202 fC	15---21	10 fC/bin
1	202 fC --- 262 fC	22---25	15 fC/bin
1	262 fC --- 322 fC	26---28	20 fC/bin
1	322 fC --- 397 fC	29---31	25 fC/bin
2	347 fC --- 722 fC	0---14	25 fC/bin
2	722 fC --- 1072 fC	15---21	50 fC/bin
2	1072 fC --- 1372 fC	22---25	75 fC/bin
2	1372 fC --- 1672 fC	26---28	100 fC/bin
2	1672 fC --- 2047 fC	29---31	125 fC/bin
3	1797 fC --- 3672 fC	0---14	125 fC/bin
3	3672 fC --- 5422 fC	15---21	250 fC/bin
3	5422 fC --- 6922 fC	22---25	375 fC/bin
3	6922 fC --- 8422 fC	26---28	500 fC/bin
3	8422 fC --- 10297 fC	29---31	625 fC/bin
Calibration Mode			
Forced 0	-2.333 fC ---- 10 fC	0---31	1/3 fC/Bin

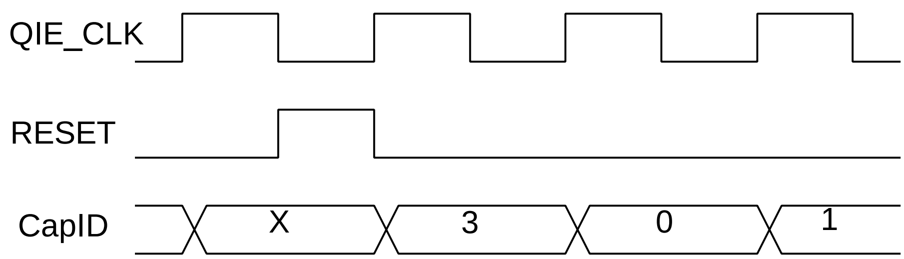
QIE Pins (Preliminary)

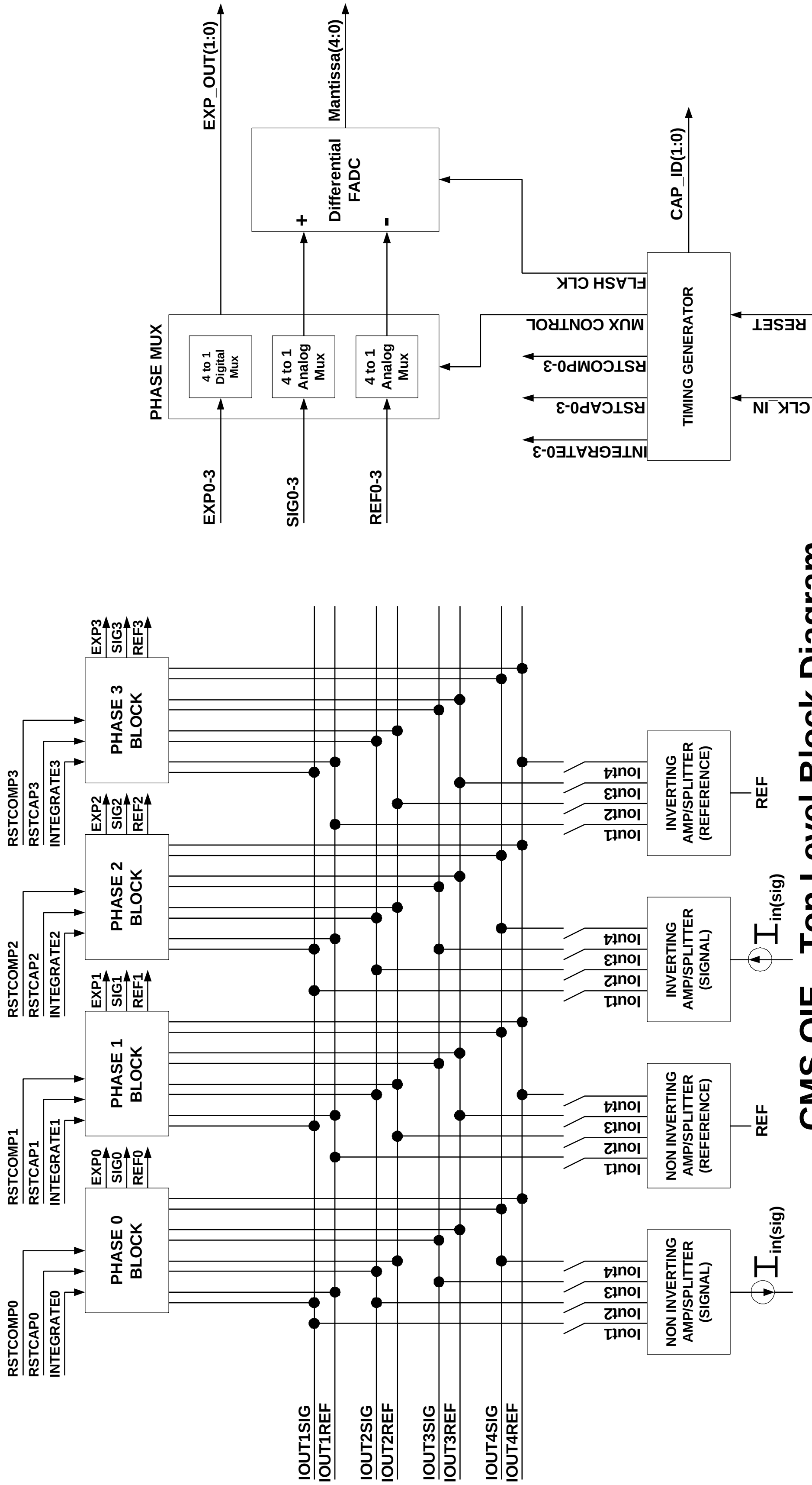
Description	# of pins
Input section	
Inverting input amp	6
Noninverting input amp	8
(Selectable impedance – ext resistor pad2)	(2)
(Selectable impedance – select bit)	(1)
Cascode GND	1
Integrators (VDD, GND, Iset, Vref)	4
Range comparators (VDD,GND)	2
FADC	
Comparators (VDD,GND)	2
Preamps (VDD,GND)	2
Bandgap Reference (VDD,GND)	2
Digital Control, I/O	
Reset and CK inputs	4
Mantissa 5 bit output	10
Exponent 2 bit output	4
Cap ID 2 bit output	4
VDD, GND, Output Iset	3
Cal/Normal Select	1
Forced Range inputs	3
Pedestal Set DAC	4
Total	60 (63)

QIE Timing Requirements for RESET

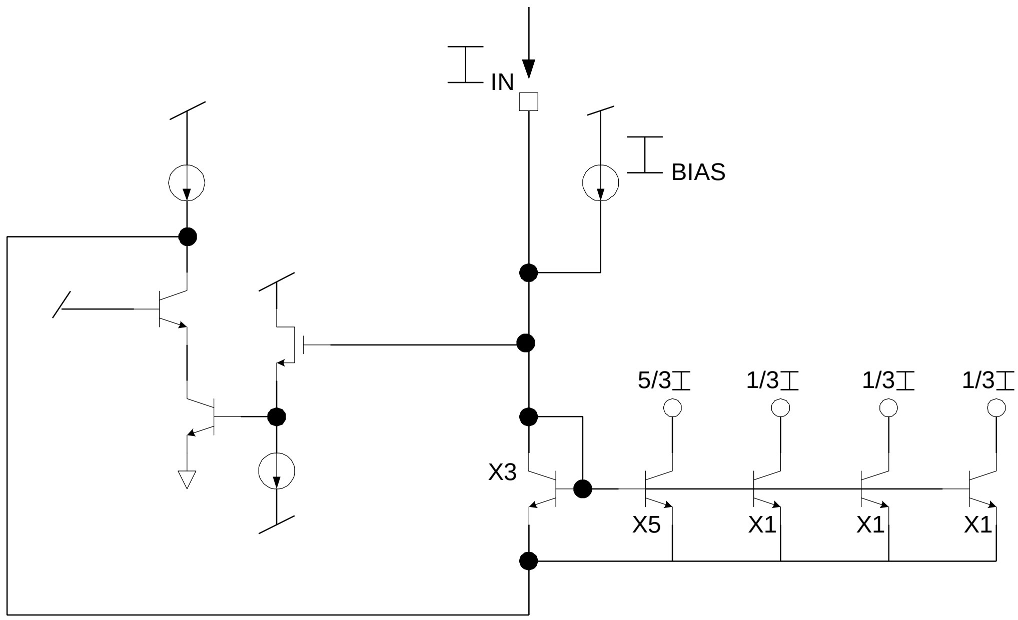
Reset must be active at the rising edge of the QIE_CLK for reset to take effect. Therefore, it is suggested that the RESET signal be activated with the falling edge of QIE_CLK and remain active until the next falling edge of QIE_CLK.

Note that the CapID resets to "3" and that the next rising edge of QIE_CLK advances the CapID to "0".

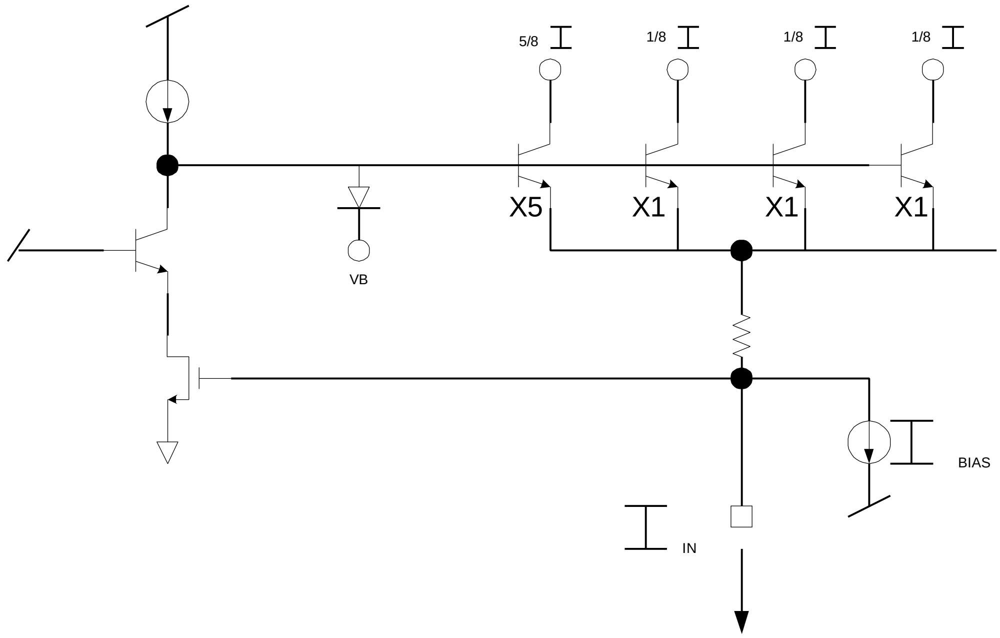




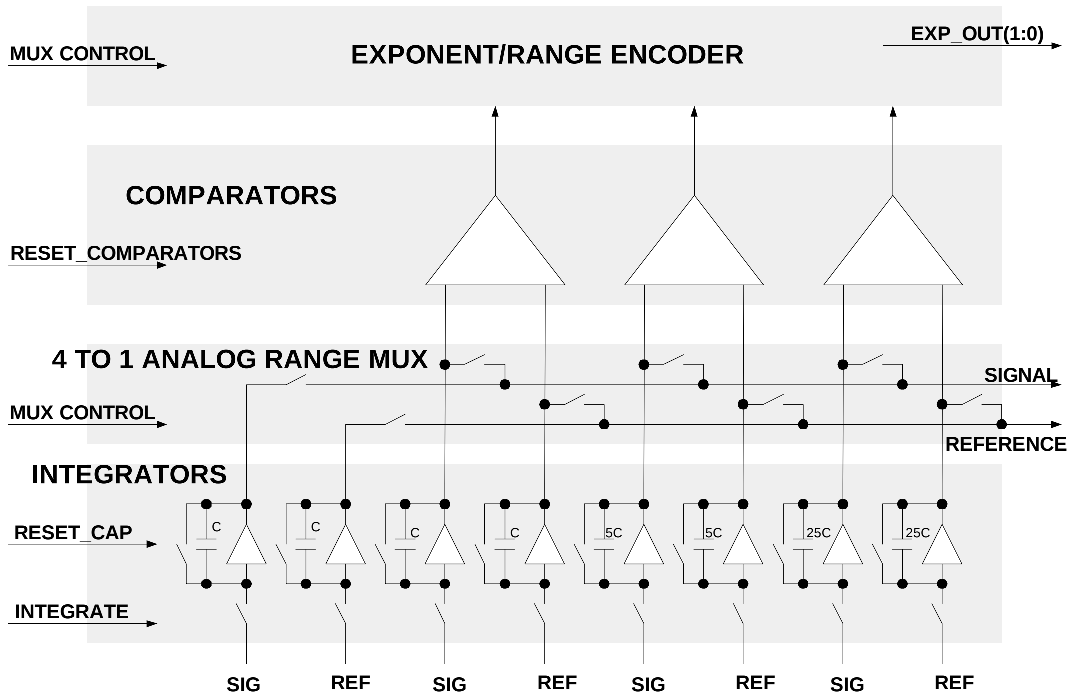
CMS QIE - Top Level Block Diagram



CMS QIE
INVERTING AMPLIFIER/SPLITTER



CMS QIE
NON-INVERTING AMPLIFIER/SPLITTER



PHASE BLOCK

A Pipelined Multiranging Integrator and Encoder ASIC for Fast Digitization of Photomultiplier Tube Signals, R. Yarema et al, Fermilab-Conf-92/148.

A Second Generation Charge Integrator and Encoder ASIC, T. Zimmerman and M. Sarraj, IEEE NS V43#3, June 1996.